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# SN74LVCH16543A 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS317M-NOVEMBER 1993-REVISED MARCH 2005

### **FEATURES**

- Member of the Texas Instruments Widebus™
   Family
- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t<sub>pd</sub> of 5.4 ns at 3.3 V
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot) > 2 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V<sub>CC</sub>)
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### DESCRIPTION/ORDERING INFORMATION

This 16-bit registered transceiver is designed for 1.65-V to 3.6-V  $\rm V_{\rm CC}$  operation.

The SN74LVCH16543A can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable (EAB or EBA) and output-enable (OEAB or OEBA) inputs are provided for each register, to permit independent control in either direction of data flow.

# DGG, DGV, OR DL PACKAGE (TOP VIEW)

|                     | _  | _      | _  |                     |
|---------------------|----|--------|----|---------------------|
| 1 <del>OEAB</del> [ | 1  | $\cup$ | 56 | 1 1 OEBA            |
| 1LEAB               | 2  |        | 55 | 1LEBA               |
| 1CEAB               | 3  |        | 54 | 1CEBA               |
| GND                 | 4  |        | 53 | GND                 |
| 1A1                 | 5  |        | 52 | 1B1                 |
| 1A2 [               | 6  |        | 51 | 1B2                 |
| v <sub>cc</sub> [   | 7  |        | 50 | ] v <sub>cc</sub>   |
| 1A3 [               | 8  |        | 49 | ] 1B3               |
| 1A4 [               | 9  |        | 48 | ] 1B4               |
| 1A5 [               | 10 |        | 47 | ] 1B5               |
| GND [               | 11 |        | 46 | ] GND               |
| 1A6 [               | 12 |        | 45 | ] 1B6               |
| 1A7 [               | 13 |        | 44 | ] 1B7               |
| 1A8 [               | 14 |        | 43 | ] 1B8               |
| 2A1                 | 15 |        | 42 | ] 2B1               |
| 2A2                 | 16 |        | 41 | 2B2                 |
| 2A3 [               | 17 |        | 40 | ] 2B3               |
| GND [               |    |        | 39 | ] GND               |
| 2A4 [               | 19 |        | 38 | ] 2B4               |
| 2A5 [               | 20 |        | 37 | ] 2B5               |
| 2A6 [               | 21 |        | 36 | ] 2B6               |
| V <sub>CC</sub>     | 22 |        | 35 | ] v <sub>cc</sub>   |
| 2A7 [               | 23 |        | 34 | 2B7                 |
| 2A8 [               | 1  |        | 33 | ] 2B8               |
| GND [               | 1  |        | 32 | ] GND               |
| 2CEAB               | 26 |        | 31 | 2CEBA               |
| 2LEAB               | 27 |        | 30 | 2LEBA               |
| 2OEAB               | 28 |        | 29 | 2 <mark>OEBA</mark> |

# **ORDERING INFORMATION**

| T <sub>A</sub> | PACKAGE <sup>(1)</sup> |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|---------------|-----------------------|------------------|
| 4000 4 0500    | SSOP – DL              | Tube          | SN74LVCH16543ADL      | LVCH16543A       |
|                | 330P – DL              | Tape and reel | SN74LVCH16543ADLR     | LVCH10543A       |
|                | TSSOP - DGG            | Tape and reel | SN74LVCH16543ADGGR    | LVCH16543A       |
| –40°C to 85°C  | TVSOP - DGV            | Tape and reel | SN74LVCH16543ADGVR    | LDH543A          |
|                | VFBGA – GQL            | Tone and real | SN74LVCH16543AGQLR    | LDH543A          |
|                | VFBGA – ZQL (Pb-free)  | Tape and reel | SN74LVCH16543AZQLR    | LDH043A          |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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SCAS317M-NOVEMBER 1993-REVISED MARCH 2005



# DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The A-to-B enable (CEAB) input must be low to enter data from A or to output data from B. If CEAB is low and LEAB is low, the A-to-B latches are transparent; a subsequent low-to-high transition of LEAB puts the A latches in the storage mode. With CEAB and OEAB both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the CEBA, LEBA, and OEBA inputs.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended. The bus-hold circuitry is part of the input circuit and is not disabled by  $\overline{\text{OE}}$  or DIR.

### **GQL OR ZQL PACKAGE** (TOP VIEW) 1 2 3 4 5 6 000000 Α 000000В С 000000 000000 D Ε $\bigcirc$ $\bigcirc$ F $\bigcirc$ $\bigcirc$ G 000000000000 Н 000000 J 000000 Κ

### **TERMINAL ASSIGNMENTS**

|   | 1     | 2                 | 3                   | 4                 | 5                 | 6                 |
|---|-------|-------------------|---------------------|-------------------|-------------------|-------------------|
| Α | 1CEAB | 1 <del>LEAB</del> | 1 <mark>OEAB</mark> | 1 <del>OEBA</del> | 1LEBA             | 1CEBA             |
| В | 1A2   | 1A1               | GND                 | GND               | 1B1               | 1B2               |
| С | 1A4   | 1A3               | V <sub>CC</sub>     | V <sub>CC</sub>   | 1B3               | 1B4               |
| D | 1A6   | 1A5               | GND                 | GND               | 1B5               | 1B6               |
| E | 1A8   | 1A7               |                     |                   | 1B7               | 1B8               |
| F | 2A1   | 2A2               |                     |                   | 2B2               | 2B1               |
| G | 2A3   | 2A4               | GND                 | GND               | 2B4               | 2B3               |
| Н | 2A5   | 2A6               | V <sub>CC</sub>     | V <sub>CC</sub>   | 2B6               | 2B5               |
| J | 2A7   | 2A8               | GND                 | GND               | 2B8               | 2B7               |
| K | 2CEAB | 2 <del>LEAB</del> | 2 <del>OEAB</del>   | 2 <del>OEBA</del> | 2 <del>LEBA</del> | 2 <del>CEBA</del> |





SCAS317M-NOVEMBER 1993-REVISED MARCH 2005

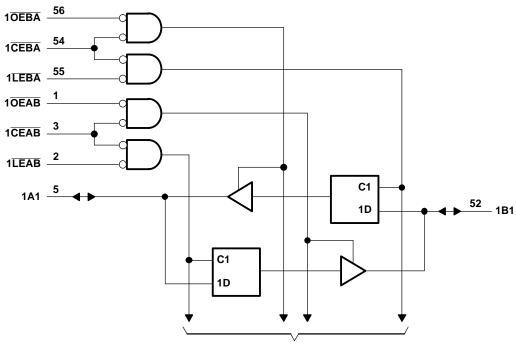
# FUNCTION TABLE<sup>(1)</sup> (EACH 8-BIT SECTION)

|      | INPUTS |      |   |                               |  |  |
|------|--------|------|---|-------------------------------|--|--|
| CEAB | LEAB   | OEAB | Α | В                             |  |  |
| Н    | Χ      | X    | Χ | Z                             |  |  |
| Х    | Χ      | Н    | Χ | Z                             |  |  |
| L    | Н      | L    | Χ | B <sub>0</sub> <sup>(2)</sup> |  |  |
| L    | L      | L    | L | L                             |  |  |
| L    | L      | L    | Н | Н                             |  |  |

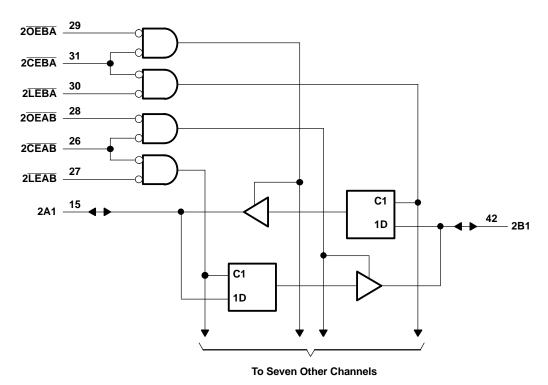
- (1) A-to-B data flow is shown; B-to-A flow control is the same, except that it uses CEBA, LEBA, and OEBA.
   (2) Output level before the indicated steady-state input conditions were
- established



# **LOGIC DIAGRAM (POSITIVE LOGIC)**



To Seven Other Channels



Pin numbers shown are for the DGG, DGV, and DL packages.



# **SN74LVCH16543A 16-BIT REGISTERED TRANSCEIVER**

SCAS317M-NOVEMBER 1993-REVISED MARCH 2005

# Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|                  |  |                         | MIN  | MAX                   | UNIT     |
|------------------|--|-------------------------|------|-----------------------|----------|
| $V_{CC}$         | Supply voltage range   |                         | -0.5 | 6.5                   | <b>V</b> |
| VI               | Input voltage range <sup>(2)</sup>   |                         | -0.5 | 6.5                   | V        |
| Vo               | Voltage range applied to any output in the high-impedance or power-off state (2) |                         | -0.5 | 6.5                   | V        |
| Vo               | Voltage range applied to any output in the high or low                           | state <sup>(2)(3)</sup> | -0.5 | V <sub>CC</sub> + 0.5 | V        |
| I <sub>IK</sub>  | Input clamp current  | V <sub>I</sub> < 0      |      | -50                   | mA       |
| I <sub>OK</sub>  | Output clamp current   | V <sub>O</sub> < 0      |      | -50                   | mA       |
| Io               | Continuous output current  |                         |      | ±50                   | mA       |
|                  | Continuous current through each V <sub>CC</sub> or GND                           |                         |      | ±100                  | mA       |
|                  |  | DGG package             |      | 64                    |          |
| 0                | Decke so the small impedance (4)   | DGV package             |      | 48                    | °C/W     |
| $\theta_{JA}$    | Package thermal impedance (4)  | DL package              |      | 56                    | -C/VV    |
|                  |  | GQL/ZQL package         |      | 42                    |          |
| T <sub>stg</sub> | Storage temperature range  |                         | -65  | 150                   | °C       |

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- The value of  $V_{\text{CC}}$  is provided in the recommended operating conditions table.
- The package thermal impedance is calculated in accordance with JESD 51-7.

# Recommended Operating Conditions<sup>(1)</sup>

|                 |                                    |  | MIN                  | MAX                  | UNIT |
|-----------------|------------------------------------|--|----------------------|----------------------|------|
| \/              | Cumply valtage                     | Operating                                  | 1.65                 | 3.6                  | V    |
| V <sub>CC</sub> | Supply voltage                     | Data retention only                        | 1.5                  |                      | V    |
|                 |                                    | V <sub>CC</sub> = 1.65 V to 1.95 V         | $0.65 \times V_{CC}$ |                      |      |
| $V_{IH}$        | High-level input voltage           | V <sub>CC</sub> = 2.3 V to 2.7 V           | 1.7                  |                      | V    |
|                 |                                    | V <sub>CC</sub> = 2.7 V to 3.6 V           | 2                    |                      |      |
|                 |                                    | V <sub>CC</sub> = 1.65 V to 1.95 V         |                      | $0.35 \times V_{CC}$ |      |
| V <sub>IL</sub> | Low-level input voltage            | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ |                      | 0.7                  | V    |
|                 |                                    | V <sub>CC</sub> = 2.7 V to 3.6 V           |                      | 0.8                  |      |
| $V_{I}$         | Input voltage                      |  | 0                    | 5.5                  | V    |
| \/              | Output voltage                     | High or low state                          | 0                    | V <sub>CC</sub>      | V    |
| Vo              | Output voltage                     | 3-state                                    | 0                    | 5.5                  | V    |
|                 |                                    | V <sub>CC</sub> = 1.65 V                   |                      | -4                   |      |
|                 | High level output ourrent          | V <sub>CC</sub> = 2.3 V                    |                      | -8                   | mA   |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 2.7 V                    |                      | -12                  | ША   |
|                 |                                    | V <sub>CC</sub> = 3 V                      |                      | -24                  |      |
|                 |                                    | V <sub>CC</sub> = 1.65 V                   |                      | 4                    |      |
|                 | Low level output ourrent           | V <sub>CC</sub> = 2.3 V                    |                      | 8                    | mA   |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 2.7 V                    |                      | 12                   | IIIA |
|                 |                                    | V <sub>CC</sub> = 3 V                      |                      | 24                   |      |
| Δt/Δν           | Input transition rise or fall rate |  |                      | 10                   | ns/V |
| $T_A$           | Operating free-air temperature     |  | -40                  | 85                   | °C   |

All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# **SN74LVCH16543A 16-BIT REGISTERED TRANSCEIVER** WITH 3-STATE OUTPUTS

SCAS317M-NOVEMBER 1993-REVISED MARCH 2005



# **Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

| P                    | ARAMETER       | TEST CONDITIONS  | V <sub>cc</sub> | MIN                   | TYP <sup>(1)</sup> MAX | UNIT |  |
|----------------------|----------------|--|-----------------|-----------------------|------------------------|------|--|
|                      |                | $I_{OH} = -100 \mu A$  | 1.65 V to 3.6 V | V <sub>CC</sub> - 0.2 |                        |      |  |
|                      |                | $I_{OH} = -4 \text{ mA}$   | 1.65 V          | 1.2                   |                        | V    |  |
| \/                   |                | $I_{OH} = -8 \text{ mA}$   | 2.3 V           | 1.7                   |                        |      |  |
| V <sub>OH</sub>      |                | I <sub>OH</sub> = -12 mA   | 2.7 V           | 2.2                   |                        | V    |  |
|                      |                | 10H = -12 IIIA   | 3 V             | 2.4                   |                        |      |  |
|                      |                | $I_{OH} = -24 \text{ mA}$  | 3 V             | 2.2                   |                        |      |  |
|                      |                | $I_{OL} = 100 \mu A$   | 1.65 V to 3.6 V |                       | 0.2                    |      |  |
|                      |                | I <sub>OL</sub> = 4 mA   | 1.65 V          |                       | 0.45                   |      |  |
| $V_{OL}$             |                | I <sub>OL</sub> = 8 mA   | 2.3 V           |                       | 0.7                    | V    |  |
|                      |                | I <sub>OL</sub> = 12 mA  | 2.7 V           |                       | 0.4                    |      |  |
|                      |                | I <sub>OL</sub> = 24 mA  | 3 V             |                       | 0.55                   |      |  |
| $I_{\parallel}$      | Control inputs | $V_1 = 0 \text{ to } 5.5 \text{ V}$  | 3.6 V           |                       | ±5                     | μΑ   |  |
| I <sub>off</sub>     |                | $V_I$ or $V_O = 5.5 \text{ V}$   | 0               |                       | ±10                    | μΑ   |  |
|                      |                | V <sub>I</sub> = 0.58 V  | 1.65 V          | (2)                   |                        |      |  |
|                      |                | V <sub>I</sub> = 1.07 V  | 1.05 V          | (2)                   |                        | μΑ   |  |
|                      |                | V <sub>I</sub> = 0.7 V   | 2.3 V           | 45                    |                        |      |  |
| I <sub>I(hold)</sub> | A or B ports   | V <sub>I</sub> = 1.7 V   | 2.3 V           | -45                   |                        |      |  |
|                      |                | $V_1 = 0.8 \text{ V}$  | 3 V             | 75                    |                        |      |  |
|                      |                | V <sub>I</sub> = 2 V   | 3 V             | -75                   |                        |      |  |
|                      |                | $V_1 = 0 \text{ to } 3.6 \text{ V}^{(3)}$  | 3.6 V           |                       | ±500                   |      |  |
| $I_{OZ}^{(4)}$       |                | $V_O = 0 \text{ V or } (V_{CC} \text{ to } 5.5 \text{ V})$   | 2.3 V to 3.6 V  |                       | ±5                     | μΑ   |  |
|                      |                | $V_I = V_{CC}$ or GND, $I_O = 0$   | 3.6 V           |                       | 20                     |      |  |
| I <sub>CC</sub>      |                | $3.6 \text{ V} \le \text{V}_{\text{I}} \le 5.5 \text{ V}^{(5)}, \qquad \qquad \text{I}_{\text{O}} = 0$ | 3.0 V           | 2                     |                        | μΑ   |  |
| $\Delta I_{CC}$      |                | One input at $V_{CC}-\ 0.6\ V$ , Other inputs at $V_{CC}$ or GND                                       | 2.7 V to 3.6 V  |                       | 500                    | μΑ   |  |
| Ci                   | Control inputs | $V_I = V_{CC}$ or GND  | 3.3 V           |                       | 5                      | pF   |  |
| C <sub>io</sub>      | A or B ports   | $V_O = V_{CC}$ or GND  | 3.3 V           |                       | 8                      | рF   |  |

# **Timing Requirements**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

|                 |                                   | $V_{CC} = 1.8 \text{ V} $ $V_{CC} = 2.5 \text{ V} $ $\pm 0.15 \text{ V} $ $0.2 \text{ V} $ |     | V <sub>CC</sub> = | 2.7 V | $V_{CC}$ = 3.3 V $\pm$ 0.3 V |     | UNIT |     |    |
|-----------------|-----------------------------------|--|-----|-------------------|-------|------------------------------|-----|------|-----|----|
|                 |                                   | MIN  | MAX | MIN               | MAX   | MIN                          | MAX | MIN  | MAX |    |
| t <sub>w</sub>  | Pulse duration, LE or CE low      | (1)  |     | (1)               |       | 3.3                          |     | 3.3  |     | ns |
| t <sub>su</sub> | Setup time, data before LE or CE↓ | (1)  |     | (1)               |       | 1.1                          |     | 1.1  |     | ns |
| t <sub>h</sub>  | Hold time, data after LE or CE↓   | (1)  |     | (1)               |       | 1.9                          |     | 1.9  |     | ns |

<sup>(1)</sup> This information was not available at the time of publication.

All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C. This information was not available at the time of publication.

This is the bus-hold maximum dynamic current required to switch the input from one state to another.

For the total leakage current in an I/O port, consult the  $I_{I(hold)}$  specification for the input voltage condition,  $0 \text{ V} < V_I < V_{CC}$ , and the  $I_{OZ}$  specification for the input voltage conditions,  $V_I = 0 \text{ V}$  or  $V_I = V_{CC}$  to 5.5 V. The bus-hold current, at input voltage greater than  $V_{CC}$ , is negligible.

This applies in the disabled state only.





# **Switching Characteristics**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | V <sub>CC</sub> = 1.8 V<br>± 0.15 V |     | $V_{CC}$ = 2.5 V $\pm$ 0.2 V |     | V <sub>CC</sub> = 2.7 V |     | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |     | UNIT |
|------------------|-----------------|----------------|-------------------------------------|-----|------------------------------|-----|-------------------------|-----|------------------------------------|-----|------|
|                  | (INPOT)         | (001F01)       | MIN                                 | MAX | MIN                          | MAX | MIN                     | MAX | MIN                                | MAX |      |
|                  | A or B          | B or A         | (1)                                 | (1) | (1)                          | (1) |                         | 6.1 | 1.2                                | 5.4 |      |
| t <sub>pd</sub>  | ĪĒ              | A or B         | (1)                                 | (1) | (1)                          | (1) |                         | 7.4 | 1.5                                | 6.1 | ns   |
| t <sub>en</sub>  | CE              | A == D         | (1)                                 | (1) | (1)                          | (1) |                         | 7.9 | 1.2                                | 6.6 | 20   |
| t <sub>dis</sub> |                 |                | AUB                                 | (1) | (1)                          | (1) | (1)                     |     | 7.1                                | 1.5 | 6.6  |
| t <sub>en</sub>  | ŌĒ              | A or D         | (1)                                 | (1) | (1)                          | (1) |                         | 7.6 | 1                                  | 6.3 |      |
| t <sub>dis</sub> | UE              | A or B         | (1)                                 | (1) | (1)                          | (1) |                         | 6.9 | 1.5                                | 6.3 | ns   |

<sup>(1)</sup> This information was not available at the time of publication.

# **Operating Characteristics**

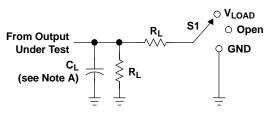
 $T_A = 25^{\circ}C$ 

| PARAMETER                     |                 |                             | TEST<br>CONDITIONS | V <sub>CC</sub> = 1.8 V<br>TYP | V <sub>CC</sub> = 2.5 V<br>TYP | V <sub>CC</sub> = 3.3 V<br>TYP | UNIT |
|-------------------------------|-----------------|-----------------------------|--------------------|--------------------------------|--------------------------------|--------------------------------|------|
| Power dissipation capacitance |                 | Outputs enabled             | f _ 10 MHz         | (1)                            | (1)                            | 44                             | nE   |
| $C_{pd}$                      | per transceiver | Outputs disabled f = 10 MHz |                    | (1)                            | (1)                            | 4                              | рЬ   |

<sup>(1)</sup> This information was not available at the time of publication.



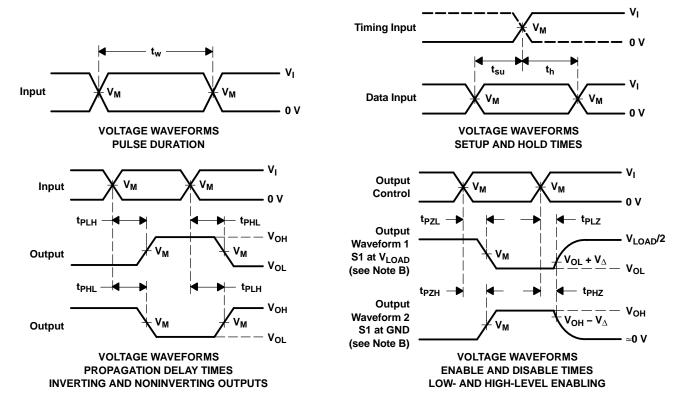
### PARAMETER MEASUREMENT INFORMATION



| TEST                               | S1                |
|------------------------------------|-------------------|
| t <sub>PLH</sub> /t <sub>PHL</sub> | Open              |
| t <sub>PLZ</sub> /t <sub>PZL</sub> | V <sub>LOAD</sub> |
| t <sub>PHZ</sub> /t <sub>PZH</sub> | GND               |

**LOAD CIRCUIT** 

| v                 | INF             | INPUTS                         |                    | V                 | •     |                | .,         |  |
|-------------------|-----------------|--------------------------------|--------------------|-------------------|-------|----------------|------------|--|
| V <sub>CC</sub>   | VI              | t <sub>r</sub> /t <sub>f</sub> | V <sub>M</sub>     | V <sub>LOAD</sub> | CL    | R <sub>L</sub> | $V_\Delta$ |  |
| 1.8 V ± 0.15 V    | V <sub>CC</sub> | ≤2 ns                          | V <sub>CC</sub> /2 | 2×V <sub>CC</sub> | 30 pF | <b>1 k</b> Ω   | 0.15 V     |  |
| 2.5 V $\pm$ 0.2 V | V <sub>CC</sub> | ≤2 ns                          | V <sub>CC</sub> /2 | 2×V <sub>CC</sub> | 30 pF | 500 Ω          | 0.15 V     |  |
| 2.7 V             | 2.7 V           | ≤2.5 ns                        | 1.5 V              | 6 V               | 50 pF | 500 Ω          | 0.3 V      |  |
| 3.3 V $\pm$ 0.3 V | 2.7 V           | ≤2.5 ns                        | 1.5 V              | 6 V               | 50 pF | 500 Ω          | 0.3 V      |  |



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω.
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
- G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

# PACKAGE OPTION ADDENDUM





### **PACKAGING INFORMATION**

| Orderable Device   | Status <sup>(1)</sup> | Package<br>Type                  | Package<br>Drawing | Pins | Package<br>Qty | e Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|--------------------|-----------------------|----------------------------------|--------------------|------|----------------|---------------------------|------------------|------------------------------|
| 74LVCH16543ADGGRE4 | ACTIVE                | TSSOP                            | DGG                | 56   | 2000           | Green (RoHS & no Sb/Br)   | CU NIPDAU        | Level-1-260C-UNLIM           |
| 74LVCH16543ADGGRG4 | ACTIVE                | TSSOP                            | DGG                | 56   | 2000           | Green (RoHS & no Sb/Br)   | CU NIPDAU        | Level-1-260C-UNLIM           |
| 74LVCH16543ADGVRE4 | ACTIVE                | TVSOP                            | DGV                | 56   | 2000           | Green (RoHS & no Sb/Br)   | CU NIPDAU        | Level-1-260C-UNLIM           |
| 74LVCH16543ADGVRG4 | ACTIVE                | TVSOP                            | DGV                | 56   | 2000           | Green (RoHS & no Sb/Br)   | CU NIPDAU        | Level-1-260C-UNLIM           |
| 74LVCH16543ADLRG4  | ACTIVE                | SSOP                             | DL                 | 56   | 1000           | Green (RoHS & no Sb/Br)   | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LVCH16543ADGGR | ACTIVE                | TSSOP                            | DGG                | 56   | 2000           | Green (RoHS & no Sb/Br)   | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LVCH16543ADGVR | ACTIVE                | TVSOP                            | DGV                | 56   | 2000           | Green (RoHS & no Sb/Br)   | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LVCH16543ADL   | ACTIVE                | SSOP                             | DL                 | 56   | 20             | Green (RoHS & no Sb/Br)   | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LVCH16543ADLG4 | ACTIVE                | SSOP                             | DL                 | 56   | 20             | Green (RoHS & no Sb/Br)   | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LVCH16543ADLR  | ACTIVE                | SSOP                             | DL                 | 56   | 1000           | Green (RoHS & no Sb/Br)   | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LVCH16543AGQLR | NRND                  | BGA MI<br>CROSTA<br>R JUNI<br>OR | GQL                | 56   | 1000           | TBD                       | SNPB             | Level-1-240C-UNLIM           |
| SN74LVCH16543AZQLR | ACTIVE                | BGA MI<br>CROSTA<br>R JUNI<br>OR | ZQL                | 56   | 1000           | Green (RoHS & no Sb/Br)   | SNAGCU           | Level-1-260C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the



# **PACKAGE OPTION ADDENDUM**

27-Sep-2007

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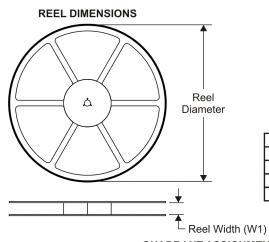
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.





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# TAPE AND REEL INFORMATION



# TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

|    | Dimension designed to accommodate the component width     |
|----|---|
|    | Dimension designed to accommodate the component length    |
|    | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device             |                                  | Package<br>Drawing |    | SPQ  | Reel<br>Diameter<br>(mm) | Reel<br>Width<br>W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1<br>(mm) | W<br>(mm) | Pin1<br>Quadrant |
|--------------------|----------------------------------|--------------------|----|------|--------------------------|--------------------------|---------|---------|---------|------------|-----------|------------------|
| SN74LVCH16543ADGGR | TSSOP                            | DGG                | 56 | 2000 | 330.0                    | 24.4                     | 8.6     | 15.6    | 1.8     | 12.0       | 24.0      | Q1               |
| SN74LVCH16543ADGVR | TVSOP                            | DGV                | 56 | 2000 | 330.0                    | 24.4                     | 6.8     | 11.7    | 1.6     | 12.0       | 24.0      | Q1               |
| SN74LVCH16543ADLR  | SSOP                             | DL                 | 56 | 1000 | 330.0                    | 32.4                     | 11.35   | 18.67   | 3.1     | 16.0       | 32.0      | Q1               |
| SN74LVCH16543AGQLR | BGA MI<br>CROSTA<br>R JUNI<br>OR | GQL                | 56 | 1000 | 330.0                    | 16.4                     | 4.8     | 7.3     | 1.45    | 8.0        | 16.0      | Q1               |
| SN74LVCH16543AZQLR | BGA MI<br>CROSTA<br>R JUNI<br>OR | ZQL                | 56 | 1000 | 330.0                    | 16.4                     | 4.8     | 7.3     | 1.45    | 8.0        | 16.0      | Q1               |



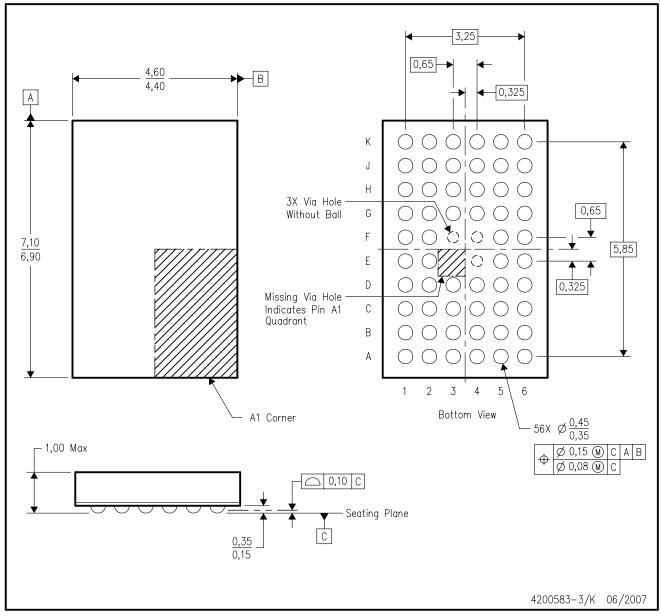


\*All dimensions are nomina

| All ullilensions are nominal |                         |                 |      |      |             |            |             |
|------------------------------|-------------------------|-----------------|------|------|-------------|------------|-------------|
| Device                       | Package Type            | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
| SN74LVCH16543ADGGR           | TSSOP                   | DGG             | 56   | 2000 | 346.0       | 346.0      | 41.0        |
| SN74LVCH16543ADGVR           | TVSOP                   | DGV             | 56   | 2000 | 346.0       | 346.0      | 41.0        |
| SN74LVCH16543ADLR            | SSOP                    | DL              | 56   | 1000 | 346.0       | 346.0      | 49.0        |
| SN74LVCH16543AGQLR           | BGA MICROSTAR<br>JUNIOR | GQL             | 56   | 1000 | 346.0       | 346.0      | 33.0        |
| SN74LVCH16543AZQLR           | BGA MICROSTAR<br>JUNIOR | ZQL             | 56   | 1000 | 346.0       | 346.0      | 33.0        |

# GQL (R-PBGA-N56)

# PLASTIC BALL GRID ARRAY



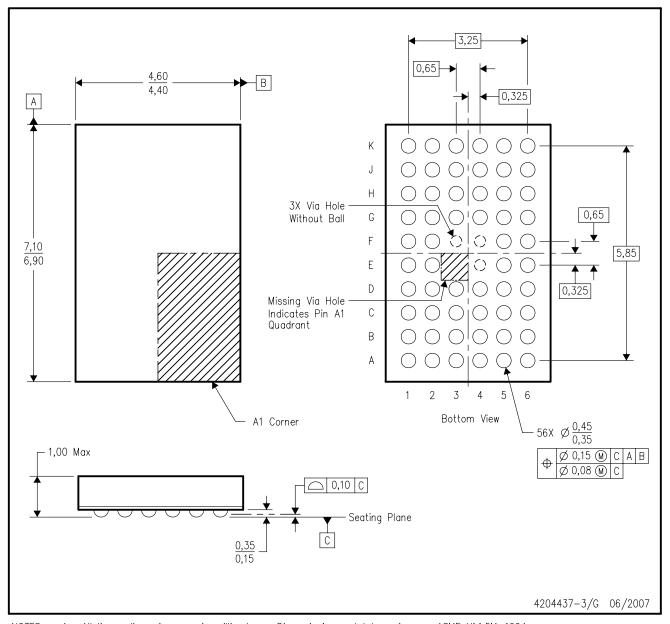
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-285 variation BA-2.
- D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.



# ZQL (R-PBGA-N56)

# PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-285 variation BA-2.
- D. This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).



# DGG (R-PDSO-G\*\*)

# PLASTIC SMALL-OUTLINE PACKAGE

### **48 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

# DL (R-PDSO-G\*\*)

# **48 PINS SHOWN**

# PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118

# DGV (R-PDSO-G\*\*)

# **24 PINS SHOWN**

# **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194

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